What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a first and second crystallographic orientation axes;

a first type of transistor formed in the semiconductor substrate having a channel region aligned along the first crystallographic orientation axis; and

a second type of transistor formed in the semiconductor substrate having a channel region aligned along the second crystallographic orientation axis and offset from the first type of transistor by an offset angle.

2. The device of claim 1, wherein the channel region of the first type of transistor has improved channel mobility from applied strain along the first crystallographic orientation axis and wherein the channel region of the second type of transistor has improved channel mobility from applied strain along the second crystallographic orientation axis.

3. The device of claim 1, wherein the first type of transistor is p-type and the second type of transistor is n-type.

4. The device of claim 3, wherein the first crystallographic orientation axis is <110> and the second crystallographic orientation axis is <100>.

5. The device of claim 1, wherein the first type of transistor is n-type and the second type of transistor is p-type.

6. The device of claim 1, wherein the offset angle is 45 degrees.

7. The device of claim 4, wherein an epitaxial layer of silicon-germanium is formed on the channel region of the first type of transistor to apply a compressive strain to the channel region along the <110> crystallographic orientation axis.

8. The device of claim 7, wherein a layer of carbon doped silicon is formed on the channel region of the second type of transistor to apply a tensile strain to the channel region along the <100> crystallographic orientation axis.

9. A method of fabricating a semiconductor device comprising:

forming PMOS devices on a semiconductor substrate with source to drain channel regions along a first crystallographic orientation axis of the semiconductor substrate;

forming NMOS devices on the semiconductor substrate with source to drain channel regions rotated by an offset angle from the source to drain channel regions of the PMOS devices to lie along a second crystallographic orientation axis of the semiconductor substrate;

applying a compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility; and

applying a tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility.

10. The method of claim 9, wherein the crystallographic orientation axis on which the PMOS devices are formed is <110> and wherein the semiconductor substrate is silicon.

11. The method of claim 9, wherein the crystallographic orientation axis on which the NMOS devices are formed is <100>.

12. The method of claim 9, wherein the offset angle with which the source to drain channel region of the NMOS devices are formed is 45 degrees.

13. The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises applying uniaxial compressive strain.

14. The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises applying biaxial compressive strain.

15. The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises:

performing a recess etch of the source to drain channel regions; and

depositing a silicon-germanium epitaxial layer on the source to drain channel regions to introduce the compressive stress to the source to drain channel regions.

16. The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility comprises applying biaxial tensile stress.

17. The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility comprises:

performing a recess etch of the source to drain channel regions; and

depositing a carbon doped silicon layer on the source to drain channel regions to introduce the tensile stress to the source to drain channel regions.

18. The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility comprises forming an interlayer dielectric layer over the NMOS devices to introduce the compressive stress to the source to drain channel regions.

19. A method of generating a layout of a semiconductor device having improved channel mobility comprising:

selecting a semiconductor substrate;

obtaining an n-type piezoresistive coefficient for n-type transistor devices and a p-type piezoresistive coefficient for p-type transistor devices by analyzing piezoresistive values associated with the semiconductor substrate;

selecting an n-type crystallographic orientation axis for the n-type transistor devices based on the obtained n-type piezoresistive coefficient;

selecting a p-type crystallographic orientation axis for the p-type transistor devices based upon the obtained p-type piezoresistive coefficient;

aligning channel regions of the n-type transistors with the n-type crystallographic orientation axis; and

aligning channel regions of the p-type transistors with the p-type crystallographic orientation axis.

20. The method of claim 19, further comprising selecting an offset angle for the channel regions of the p-type transistors from the channel regions of the n-type transistors.

21. The method of claim 18, wherein obtaining the n-type piezoresistive coefficient comprises identifying a minimum piezoresistive value as the coefficient.

22. The method of claim 18, wherein obtaining the p-type piezoresistive coefficient comprises identifying a maximum piezoresistive value as the coefficient.

23. The method of claim 18, further comprising fabricating a semiconductor device with the layout and introducing tensile strain on the channel regions of the n-type transistors and compressive strain on the channel regions of the p-type transistors.